Jitter measurements on OC-48 optical transceivers using the OmniBER 718 or OmniBER 725

Product Note

Agilent Technologies

Introduction

Optical transceivers used in high-speed digital communication systems are typically required to meet a specific set of performance levels. Synchronous networks such as the Synchronous Digital Hierarchy (SDH) and the Synchronous Optical NETwork (SONET) rely on highly accurate and stable synchronisation to process data in and out of network elements. Any phase variations or jitter induced in the network will cause a degradation of transmission quality, bit errors and data loss. Therefore, it is important to understand jitter and its impact on network performance.
Jitter is used to describe short term, non-cumulative variations of the significant instants of a digital signal from their ideal positions in time. Although definitions and specifications are described by industry standards, test methodologies are usually left to the end user. Historically, it has been difficult to achieve accurate and repeatable jitter measurements.

This note focuses on jitter measurements of single-mode optical transceivers used in SONET/SDH networks using the OmniBER 718/725. The purpose is to describe jitter and the intent of the different measurements including jitter generation, tolerance and transfer. Measurement methods and the advantages of using the OmniBER 718/725 are considered for each type of jitter measurement, test methodology and results are discussed.

The note is divided into several sections:

- Definition of jitter
- Jitter specifications for SONET/SDH
- Test methods to measure jitter
- Jitter measurements of OC-48 transceivers

What is jitter?

Jitter is the term used to describe short term, non cumulative variations at the significant instants of a digital signal that arise either too late or too early when compared to their ideal position in time. For example, the significant instant can be the rising or the falling edge of a pulse. Figure 1 shows a jittered signal viewed at different instants. The jitter function is represented by the jitter magnitude of the variations of the significant instants over time.
Wander is closely related to jitter and generally refers to long term variations in the significant instants. Phase variations corresponding to frequencies below 10 Hz are normally called wander.

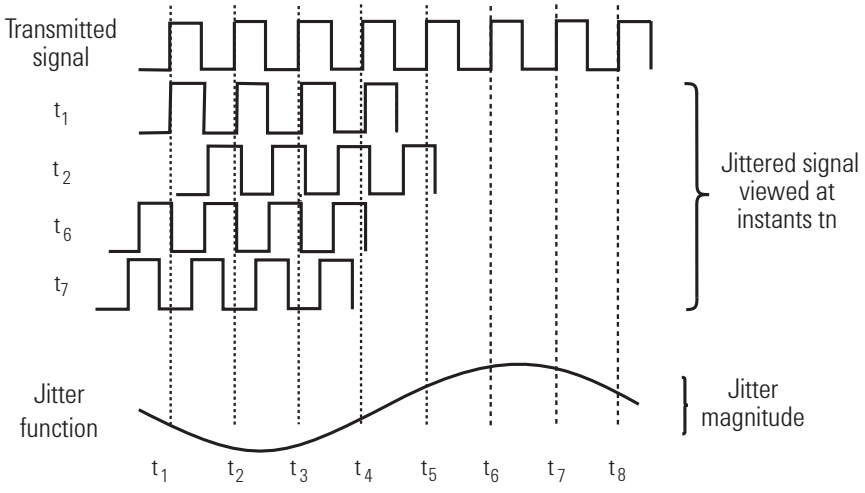


Figure 1. Jittered signal viewed at different instants.

Sources of jitter

A synchronous network such as SONET or SDH can have two main sources of jitter:

- Intrinsic jitter is directly linked to the transmitted bit pattern, and it includes effects such as Duty Cycle Distortion (DCD) and Inter Symbol Interference (ISI).
- Extrinsic jitter can be caused by multiplexers and demultiplexers during signal compensation and pointer adjustment (pointer, stuffing and mapping jitter). It can also be caused externally by crosstalk and Electro- magnetic Interference.

Duty Cycle Distortion (DCD) is the difference in the mean pulse width between a logic "1" and a logic "0". Variations of the mean pulse width cause DCD and directly impact significant instants from the ideal position in time by affecting their phase.

Inter Symbol Interference (ISI) refers to variations of the significant instants (i.e. the ideal position in time for the signal to arrive) due to Data Pattern Dependent (DPD) jitter. It is a leading cause of signal degradation as peak amplitude, rise and fall time are affected. Ultimately, ISI becomes the limiting factor for signalling rate and transmission distance as clock and data recovery circuits cannot cope with the excessive amount of jitter induced by DCD.

Figure 2 illustrates the effects of ISI and DPD on a digital signal. When different bit sequences are transmitted, variations of the peak amplitude, rise and fall times are observed. These variations can be related to the frequency content of the bit sequence propagating through the transmission media and is affected by many parameters such impedance matching, capacitance, inductance and dispersion. ISI can be minimised by careful layout and composition of a PCB and it is important to address these issues early in the design especially at higher data rate.

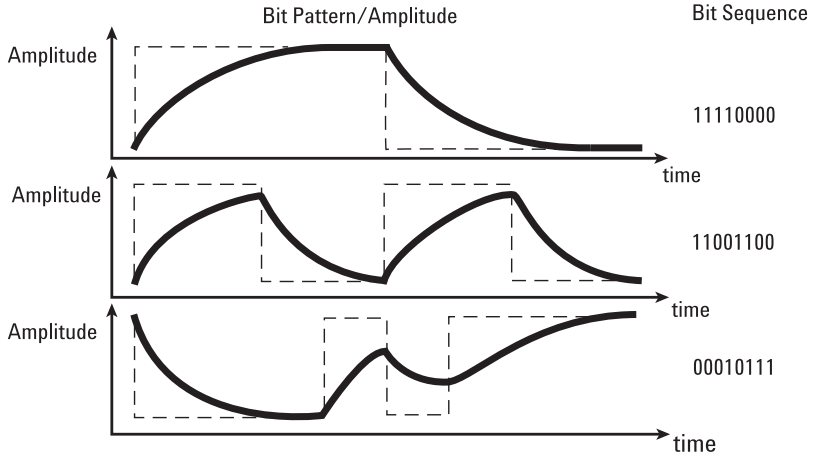


Figure 2. Influence of bit sequence on amplitude, rise and fall time.

Pointer, stuffing and mapping jitter are induced at system level during the multiplexing and demultiplexing of digital signals. Pointers are used to compensate clock differences between two networks or network elements. Depending on the multiplexing hierarchy, residual phase modulation called pointer jitter can be induced during the compensation process.

Stuffing and mapping are used to convert asynchronous digital signals into synchronous signals by inserting bits during multiplexing and removing them during demultiplexing. The residual phase modulation between the two processes is referred to as stuffing and mapping jitter.

Cross-talk is also a cause of jitter as it produces phase variations in the transmitted digital signal. It arises from magnetic field generated by nearby signals. Power supply noise and EMI also affect jitter.

Regardless of its origin, jitter always manifests itself as phase variations of the significant instants compared to their ideal positions. It is important to note that any changes in the transmission media (e.g. impedance, capacitance, inductance and dispersion) will be responsible for most of the jitter in digital transmission circuits. Therefore, when designing a PCB, care must be taken to control the effective impedance of the different elements and minimize the signal variations due to the frequency content of the transmitted bit sequence.

Disruptions caused by jitter

SONET and SDH are synchronous networks and they rely on highly accurate and stable clocks to process data in and out of network elements. It is the job of the clock recovery circuit to sample digital signals correctly. Two cases can be considered:

- Jitter frequencies are low and the clock recovery is able to track the relatively slow phase variations of the input signal. Sampling of the data occurs correctly.
- Jitter frequencies are high and the clock recovery cannot keep up with the fast phase variations of the incoming signal and data is recovered incorrectly. With large amounts of jitter, high bit rate can cause loss of frame and even loss of synchronisation.

Jitter can also accumulate in a transmission network depending on the jitter generation and transfer characteristics of the network elements.

Definition of Unit Interval (UI)

Jitter is traditionally measured in Unit Interval (UI) where one UI corresponds to the phase deviation of one clock period and is graphically illustrated in Figure 3. The percentage of jitter can be calculated using the following equation:

$$\%\text{jitter}=(T_j/T_0)\text{x}100\%$$

where T_0 is the clock period and T_j is the jitter time amplitude. One UI represents 100% jitter. It is important to note that Unit Intervals are independent of the bit rate and it is possible to compare jitter amplitude at different hierarchical levels in a network element.

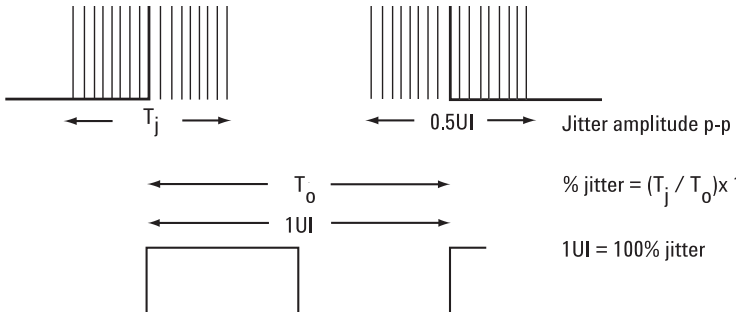


Figure 3. Graphical represntation of Unit Interval (UI).

Jitter specifications for SONET/SDH

Jitter generation

Jitter Generation is defined as the amount of jitter present at the OC-N/STS-N output of a SONET network element in the absence of applied jitter. Table 1 shows the requirements for jitter generation at different transmission rate. Two jitter parameters are defined:

- Jitter peak to peak: this is the maximum measured jitter amplitude
- Jitter rms: this is the root mean square (rms) value of the jitter signal that provides an indication of the jitter power.

OC-N/STS-N Level	f_1 (kHz)	f_2 (MHz)	Limit (UI_{ms})	Limit (UI_{p-p})
1	12	0.4	< 0.01	< 0.10
3	12	1.3	< 0.01	< 0.10
12	12	5	< 0.01	< 0.10
48	12	20	< 0.01	< 0.10
48(B)	12	20	< 0.01	< 0.10

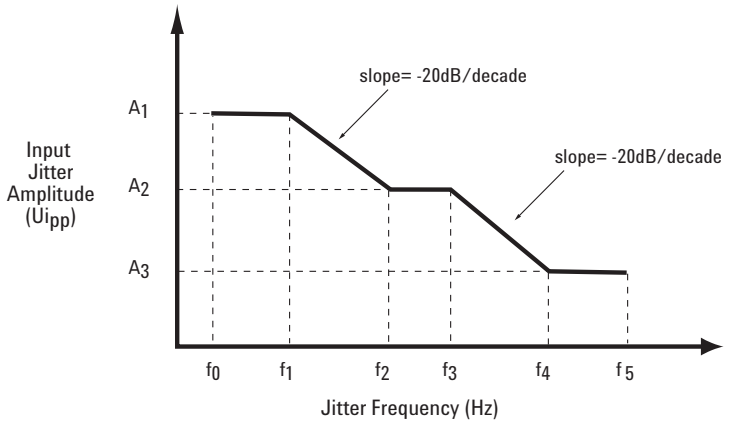
Table 1. SONET requirements for jitter generation (GR253)

These specifications apply to network elements (i.e. to the whole system) and therefore, compliance of individual components alone does not guarantee that the system will meet the SONET requirements for jitter generation. Interface between components and board layout must be carefully considered in order to minimise jitter generation.

At OC-48, the jitter generation specification requires less than 100 mUI_{p-p} and less than 10 mUI_{rms} when measured using a 12 kHz high pass and a 20 MHz low pass filter.

Jitter tolerance

Jitter Tolerance is defined as the peak to peak amplitude of sinusoidal jitter applied on the OC-N input of a network element that causes an equivalent 1dB-sensitivity penalty. Jitter Tolerance represents the ability of the CDR circuit to recover an incoming bit sequence correctly despite the applied jitter. In order to pass this requirement, network elements must exceed the limits defined in Table 2.



OC-N/STS-N Level	f_0 (Hz)	f_1 (Hz)	f_2 (Hz)	f_3 (Hz)	f_4 (Hz)	A_1 (UI_{pp})	A_2 (UI_{pp})	A_3 (UI_{pp})
1	10	30	300	2k	20k	0.15	1.5	15
3	10	30	300	6.5k	6.5k	0.15	1.5	15
12	10	30	300	25k	250k	0.15	1.5	15
48	10	600	6000	100k	1000k	0.15	1.5	15

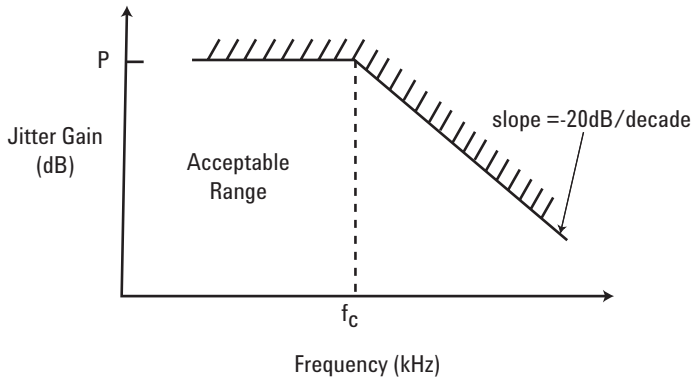
Table 2. SONET requirements for jitter tolerance.

Jitter Transfer

Jitter Transfer is defined as the ratio of jitter on the output OC-N/STS-N signal to the jitter applied on the input OC-N/STS-N signal versus frequency. The jitter transfer function is calculated using the following equation:

Jitter Transfer=20.Log(Output jitter/Input jitter)

where output and input jitter are expressed in UI and jitter transfer in dB. Jitter Transfer is comparable to a gain function where negative and positive dB indicates that the network elements attenuates and amplifies jitter respectively. Table 3 shows the SONET requirement for jitter transfer. In order to pass this requirement, network elements must not exceed the limits shown in Table 3.



OC-N/STS-N Level	f_0 (KHz)	P (dB)
1	40	0.1
3	130	0.1
12	500	0.1
48	2000	0.1

Table 3. SONET requirements for jitter transfer.

Importance of CDR circuits

It is important to understand that the ability of a network element to pass both jitter tolerance and jitter transfer is directly linked to the bandwidth of the PLL (Phase Lock Loop) used in the CDR circuit. Good jitter tolerance performance requires a clock recovery with high bandwidth so that the PLL can track the jittered input signal and still successfully recover the clock. On the other hand, jitter transfer compliance is achieved by limiting the bandwidth of the PLL to ensure that higher frequencies are not transmitted. Therefore the successful design of a CDR circuit is always a compromise between Tolerance performance and Transfer compliance.

Test methods to measure jitter

Available test methods

This section describes the most frequently encountered techniques to measure jitter: oscilloscope, phase detector and dedicated SONET/SDH jitter analyser. Each technique has its own advantages and limitations but in order to measure jitter, two main elements are required: a source that generates known amounts of jitter and a detector that accurately measures jitter. The limitations of each element must be understood to ensure the correct interpretation of the results.

Oscilloscope

Jitter can be directly measured using an oscilloscope. A typical test configuration is shown on Figure 4. This technique mainly relies on the ability to supply a jitter free trigger signal. Any jitter on the trigger signal will affect the validity of the results.

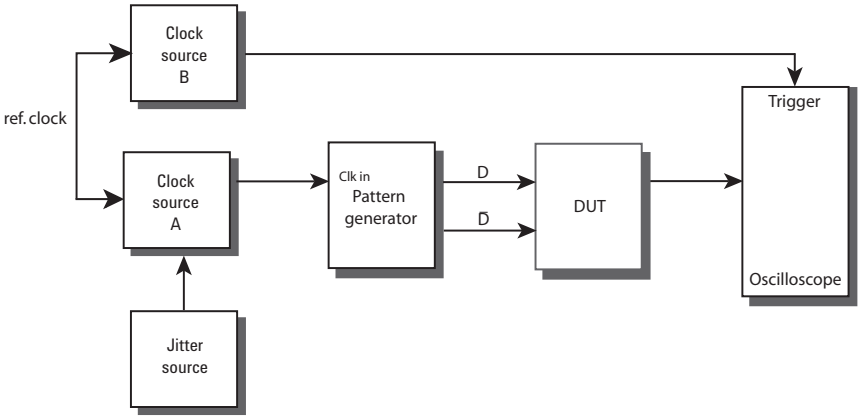


Figure 4. Test configuration using an oscilloscope

The limitations of this technique are:

- Limited to one UIp-p. Above this level, the eye diagram is totally closed.
- Large measurement bandwidth therefore noise level is usually high and no spectral information can be extracted.

Phase detector

Figure 5 shows a test configuration, based on a phase detector, which addresses most of the limitations associated with the oscilloscope technique. The phase detector compares the phase of the recovered clock from the network element with a jitter free clock source and its output is proportional to the jitter on the recovered clock. Jitter can then be measured through the appropriate band-pass filter. However, this technique still has the following limitations:

- Only function at specific data rate
- Need external filters

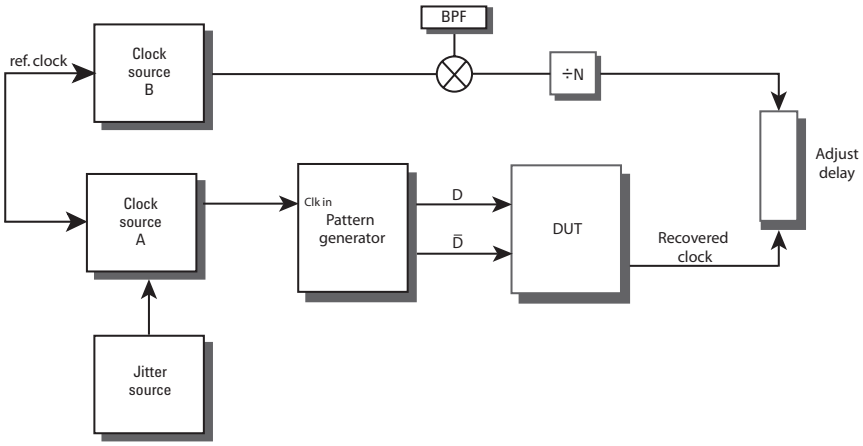


Figure 5. Test configuration based on a phase detector.

Dedicated SONET/SDH communications analyzers with jitter analysis: OmniBER 718/725

The Agilent Technologies OmniBER 718/725 communications performance analyzers (shown in Figure 6) offer single box multirate SONET/SDH testers up to 2.5Gb/s. These are ideally suited for the product test, installation, maintenance and verification of SONET/SDH transport networks and networks equipment. Both instruments provide extensive BER measurement capabilities. The OmniBER 718 can also provides additional PDH/DSn capability or in the case of the OmniBER 725 convenient Binary interfaces with SONET/SDH framed/unframed PRBS signals for component and O/E, E/O testing. In this article we will concentrate on the jitter measurement aspects of the products.

Further information and full specification of the instrument feature set is available from the specifications for OmniBER 718/725. Product numbers 37718A and J1409A.
Jitter Generation, Tolerance and Transfer measurements can be performed via the Network SONET/SDH Optical/Electrical interfaces. (also via the Binary interfaces in the case of OmniBER 725) These instruments provide comprehensive jitter capability and meet or exceed existing Telcordia GR-253 and ITU-T G.825, G.958 and O.172 standards applicable to the measurement of jitter on these networks. The transmitter uses a wide band PLL to generate known amount of jitter and the receiver is based on a very narrow band PLL in order to accurately detect and measure the jitter content of the incoming signal. Both transmitter and receiver are now described in more detail.

Figure 6. OmniBER 718/725

A simplified block diagram of the OmniBER 718 is shown in Figure 7 followed by simplified block diagrams Figures 8 and 9 of SONET/SDH signal generation and detection, jitter generation and measurement.

Simplified transmit and receive sections

Note:
The example shown is OmniBER 718, the OmniBER 725 version, does not have PDH/DSn sections, but has differential Binary Interfaces for SONET/SDH CLOCK and DATA

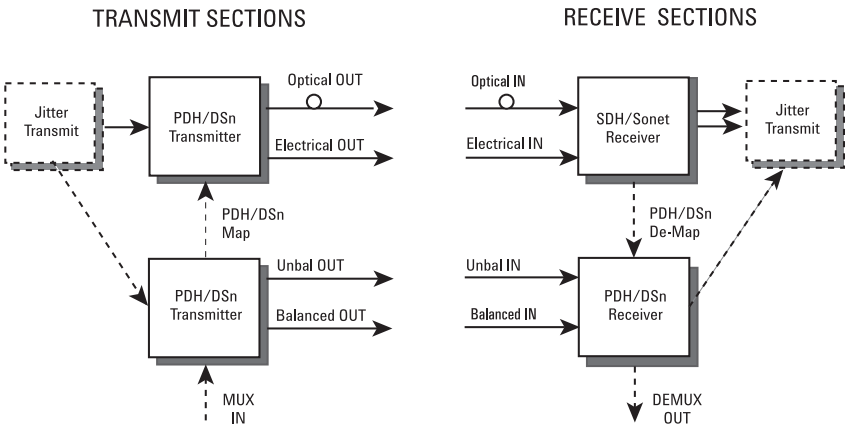


Figure 7. Simplified Block Diagram of Transmit and Receive sections.

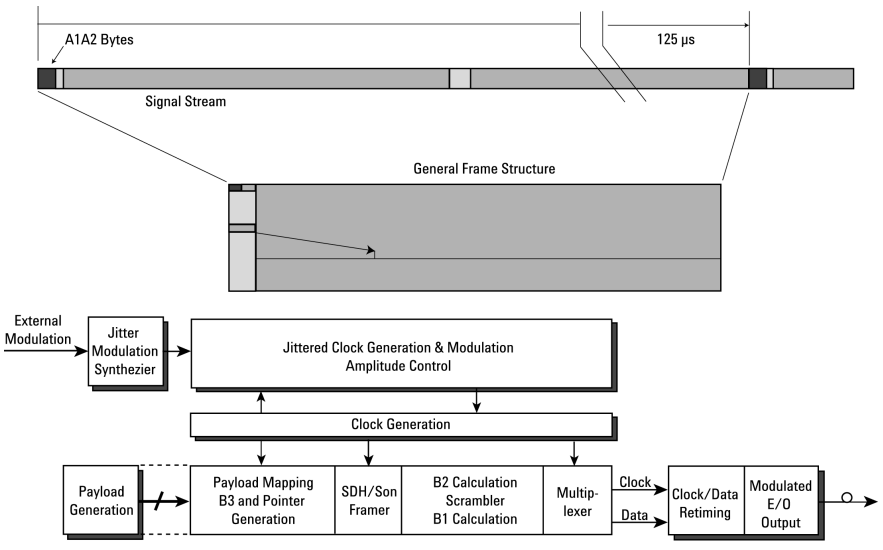


Figure 8. Simplified block diagram of generation sections

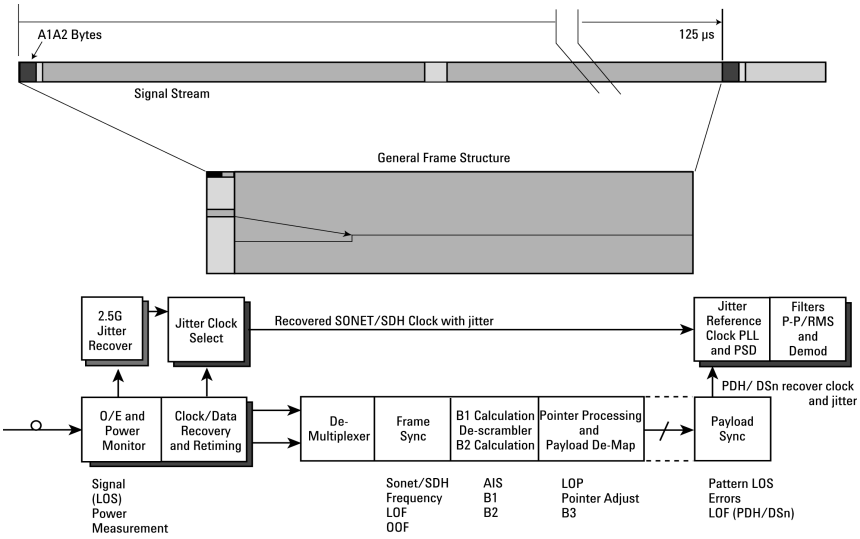


Figure 9. Simplified block diagram of receiver sections

Figure 10 shows a simplified analogue representation of a wide band PLL used to add jitter at a variety of frequencies to a Clock signal. In practice the OmniBER uses a combination of analogue and digital circuitry, and also processing techniques to accurately generate jitter over the extensive amplitudes (UI_{p-p}) and frequencies required. This jittered Clock signal is used in the generation of SONET/SDH signals with known amounts of jitter to stress the Network Element or device under test.

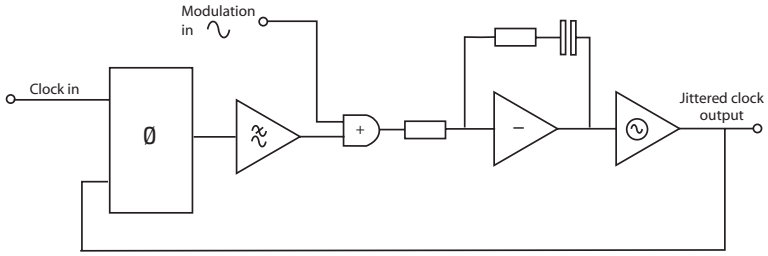


Figure 10. Basic clock operation of the jitter transmitter

The Transmitter Clock reference can be provided from a variety of Internal/ External/Recovered sources. Modulation can be also be derived internal/ external sources with Internal providing fixed and swept frequency and modulation amplitude control necessary for Jitter Transfer and Autotolerance measurements. The Clock with/without jitter is used in the subsequent generation of Framed SONET/SDH interface output signals.

In contrast to the transmitter, the receive loop, represented in much simplified form in Figure 11 has a very narrow band PLL. The main difference that gives the receiver its narrow bandwidth is the VCO or VCXO in this case. While the transmitter has a VCO which generates multi-MHz / volt gain, the receiver VCXO only moves by a few part per million in response to changes of volts on its control input.

This creates a narrow band PLL, so unresponsive to changes in its reference signal, that it generates a reference at the average frequency/phase of the jittered clock signal with phase modulation removed. This is compared with jittered clock by PSD and low-pass filtered to demodulate the jitter.

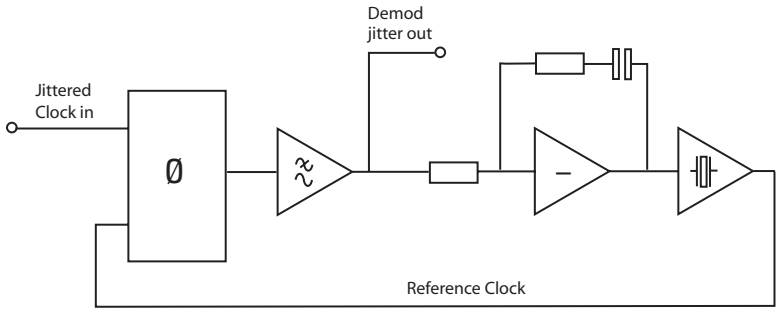


Figure 11. Basic clock operation of the jitter receiver

The Jittered Clock signal applied to the Receiver measurement section must first be derived from the SONET/SDH interface. This requires (O/E) conversion and clock recovery specifically designed to ensure jitter content of the Optical signal is carried in the Jittered Clock.

Measurement calibration

The jitter measurement method described requires the Clock to be recovered, transparently (including jitter), from the SONET/SDH signal, followed by removal of jitter from the recovered clock to create the reference for jitter measurements. To ensure optimum performance and measurement accuracy, the instrument is designed and calibrated to minimise intrinsic noise in the measurement processes. This involves extensive tests during production under a variety of signal conditions to characterise and compensate for these effects. Accuracy of jitter generation and measurement is confirmed by traceable methods using a variety of Spectrum Analysis techniques.

Jitter measurement examples on OC-48 transceivers using OmniBER 718/725

Agilent Technologies OC-48 transceivers and reference design boards are used to illustrate three different types of jitter measurements with the OmniBER 718/725. The HFCT-5402D laser based, duplex transceiver with integral clock and data recovery circuits and the HFCT-5942L is a 1300nm, laser based Small Form Factor transceiver.

These reference design boards include commercially available multiplexer, demultiplexer and CDR circuit and therefore, they are more representative of performance that would be observed at system level. Jitter generation measurements is illustrated using the HFCT-5402D and AMCC S3041/S3042 reference design. Jitter tolerance and jitter transfer measurements are illustrated using the HFCT-5942L (OC-48 LC Small Form Factor) and Vitesse VSC8122/VSC8140 reference design. For each type of jitter, test configurations are explained and test results are discussed.

General test configuration of the OmniBER 718/725

In order to accurately measure jitter, it is necessary to set the correct configuration on the OmniBER. Figure 9 shows the main settings for receiver and transmitter. Both are set to operate at 2.5 Gb/s using an STS-48C (concatenated frames) pattern with a 2^{23}-1 PRBS payload. This payload is used as it has the highest low frequency content and will therefore generate the highest amount of DPD jitter. The OmniBER has a built in optical power meter and the receiver maximum operating power is –8 dBm therefore appropriate attenuation should be used to ensure receiver is not overloaded. The recommended power level for jitter measurements is approximately -14dBm.

In the result window on Figure 12, a scale from –40 to 0 dBm is used to display the received power and three ranges can be identified:

- Out of range (red region): measurements cannot be made when the received optical power is within this range.
- BER only (green region): only BER can be measured accurately.
- BER and jitter (white region): jitter can be measured accurately when received optical power is within this region.

The received optical power must always remain within the white region when measuring jitter as optical sensitivity will affect the results.

Figure 12. OmniBER 718 screen shot and Rx and TX configuration

Jitter generation

Jitter generation measurements are illustrated using the HFCT-5402D and AMCC S3041/S3042 reference design. The AMCC S3041 and S3042 are fully integrated SONET/ SDH multiplexer demultiplexer ICs offering STS-48 interface and the complete interface between the ICs and the transceiver can be found in Agilent Technologies Application Note 1172 (SONET/SDH OC-48 Transceiver Reference Design).

Figure 13 shows the test arrangement used to measure jitter generation. Differential clock and data are fed electrically into the demultiplexer (S3042). The 8 bit parallel data is then multiplexed by S3041 and the serial differential outputs are AC coupled into the HFCT-5402D transmitter. The optical output is connected to the receiver of the OmniBER via an optical attenuator and the received optical power is set to –14.0 dBm. It is necessary to load a valid STS-48C pattern into the pattern generator to allow the OmniBER to receive a valid OC-48 framed signal and to insure that measurements are made using real traffic.

Note:
If the OmniBER 725 is used in place of the OmniBER 718 then the OmniBER 725's its 'transmit' section can be used instead of the HS-BER pattern generator. This provides AC coupled differential output ports with approximately 750mV p-p swing and appropriate external biasing can be applied if required by device under test. Note also that using the OmniBER 725 alternative avoids the need to load the STS-48C pattern required in HS-BER as this is available from the Optical or Binary ports.

It is important to ensure appropriate measurement range and correct filter BW settings are chosen when making any intrinsic Jitter measurements. The most sensitive range should be used and HP/LP filters chosen according to the specification being tested see Receiver Input settings in Figure 14.

Also, it is important to ensure the unscrambled bytes in the SONET/SDH overhead signal, for example the Z0 bytes, contain some transitions to avoid excessive 0's sequence which can affect Jitter measurements. Note the OmniBER generates the recommended sequences by default (e.g SONET uses numbered sequence, SDH contains AA55).

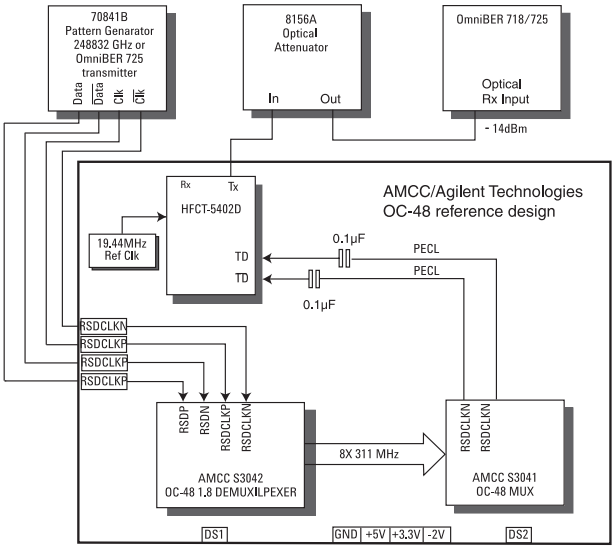


Figure 13. Test arrangement to measure jitter generation (OmniBER 725 can be used in place of OmniBER 718 and 70841B, see note above)

In order to comply with the Telcordia GR-253, jitter generation must be measured through a band-pass filter. The receiver window on Figure 14 shows that a 12 kHz high-pass and a 20 MHz low-pass filter are used. The jitter generation measurements must be performed in cumulative mode over at least a one minute period.

Figure 14. Jitter generation configuration and result (OmniBER 718 screen shot)

Jitter generation performance for the reference design is:

- 71 mUI_{p-p}
- 7 mUI_{rms}

The AMCC/Agilent Technologies reference design using HFCT5402D and S3041/S3042 passes and exceeds Telcordia GR-253 for jitter generation. It is important to remember that jitter has many potential sources and this result takes into account the contribution of the PCB, including demultiplexer, multiplexer, transceiver and board layout. It is also important that some account is taken of the expected measurement uncertainty involved in any intrinsic level broadband phase (jitter) measurement. Appropriate guard-bands should be build into the design, production and customer specifications to ensure realistic margins as p-p phase noise measurement is a random quantity. For example, it should be confirmed all parts meet required limit and also advisable to monitor result spread in production testing to confirm results have at least a 10-20% margin on the requirement.

Jitter tolerance

Jitter tolerance measurement is illustrated using the HFCT-5942L (OC-48 LC Small Form Factor) and Vitesse VSC8122/VSC8140 reference design. The evaluation board includes:

- The VSC8140, a fully integrated SONET/SDH multiplexer demultiplexer ICs offering STS-48 interface
- The VSC8122, a multi-rate clock and data recovery IC capable of STS-3/12/48 or Gigabit Ethernet rate

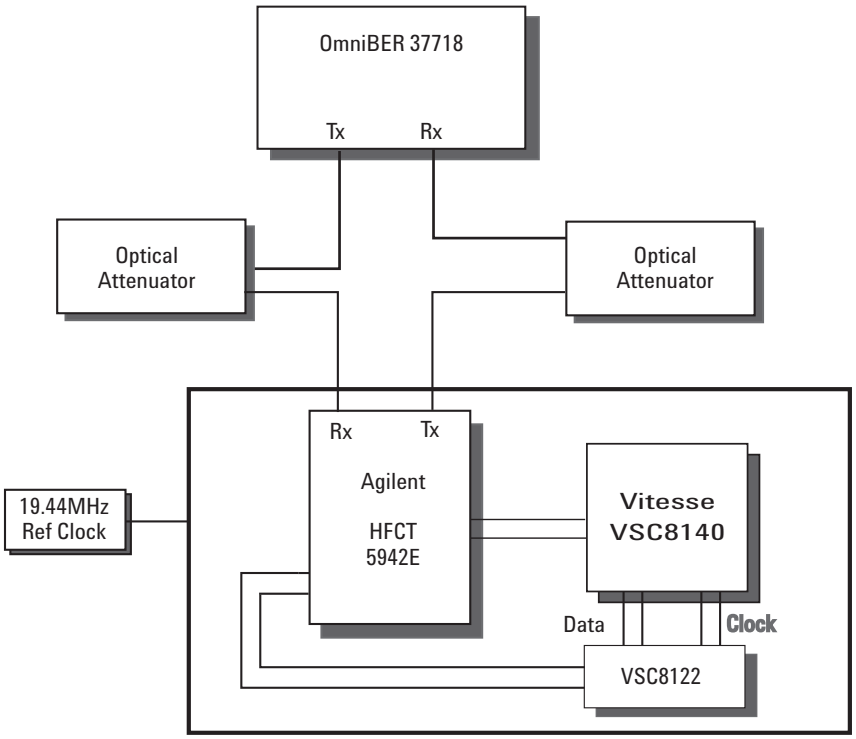


Figure 15. Test arrangement to measure jitter tolerance

Figure 15 shows the test arrangement used to measure jitter tolerance. An optical OC-48 signal is generated by the transmitter of the OmniBER and connected to the HFCT-5942L receiver via an optical attenuator. The received signal is recovered by the VSC8122, demultiplexed and multiplexed by the VSC8140 and the STS-48 electrical outputs drive the HFCT-5942L transmitter. The OC-48 signal generated is connected to the receiver of the OmniBER via an optical attenuator. The input optical power at the HFCT-5942L is set at sensitivity plus one dBm. Figure 16 shows the transmitter output window of the OmniBER 718 used to set different parameters for jitter tolerance (bit rate, pattern, and error threshold).

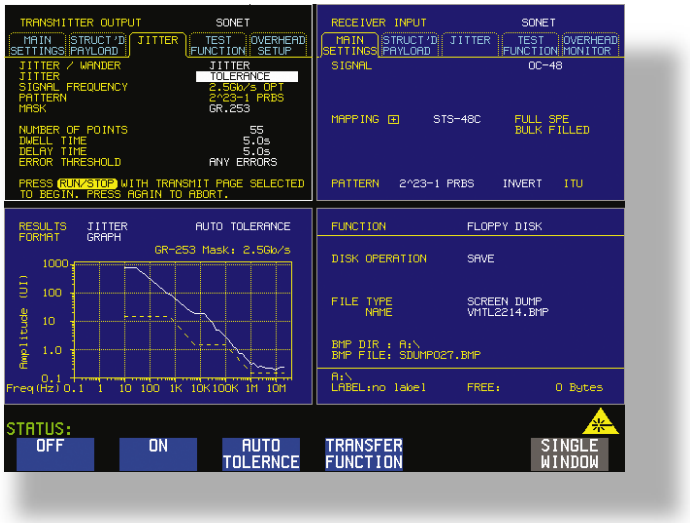


Figure 16 Jitter tolerance configuration and result (OmniBER 37728A screen shot)

The OmniBER sweeps the mask, altering jitter amplitude at each point using a binary search algorithim to find max tolerable jitter for the error threshold chosen. As each change in Amplitude/Frequency is made in this process a selectable Delay Time (to ensure UUT settlement), followed by a selectable Dwell Time (checking for errors and measuring error threshold) is applied.
The error threshold can be set for errors or error rate (related to measurement Dwell time).

The Vitesse/Agilent Technologies reference design using HFCT-5942L and VSC8122/VSC8140 passes and exceeds Telcordia GR-253 requirements for jitter tolerance. The result window of the OmniBER in Figure 16 shows that the jitter amplitude (solid line) is above the tolerance mask (dash line).
The measurement shows that the VSC8122 is able to track large amount of jitter before degrading the BER. Jitter tolerance is an important parameter as it indicates how CDR circuits perform in presence of jittered signals.

Jitter transfer

Jitter transfer measurement is illustrated using the HFCT5942L (OC-48 LC Small Form Factor) and Vitesse VSC8122/VSC8140 reference design. The test arrangement is the same as the one used for jitter tolerance and is illustrated in Figure 15.

Before measuring jitter transfer, it is necessary to perform a Back to Back calibration run of the OmnBER to normalize the Transmitter and Receiver. This is necessary because Jitter Transfer measurement accuracy needs to be better than 0.1dB therefore a very narrow BW tracking filter technique is employed. During Calibration run the OmniBER is looped back optically on itself via an optical attenuator and the input optical power is set to –14 dBm (i.e. within the white region of the built-in optical power meter). During calibration, jitter measured by the receiver is correlated to jitter generated by the transmitter. Once Calibration run is complete the instrument mode changes to Jitter Transfer Measurement mode. The unit under test is then inserted in the loopback path as in Figure 15 with appropriate attenuation, measurement is started and the Jitter Transfer is plotted.

Figure 17 shows the transmitter output window of the OmniBER used to set different parameters for jitter transfer (bit rate, mask).

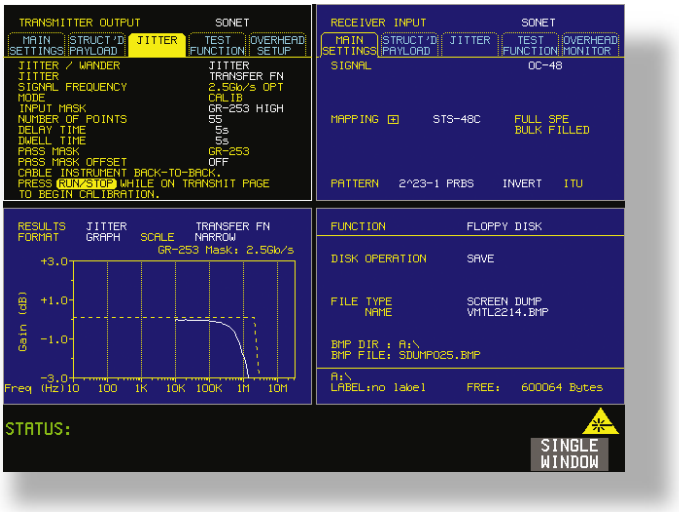


Figure 17. Jitter transfer configuration and result (OmniBER 718 screen shot)

The Vitesse/Agilent Technologies reference design using HFCT-5942L and VSC8122/VSC8140 passes and exceeds Telcordia GR-253 requirements for jitter transfer. The result window of the OmniBER in Figure 17 shows that the jitter gain (solid line) is below the transfer mask (dash line).
This measurement shows that the VSC8122 clock and data recovery does not amplify or pass though jitter over the defined frequency range and rolls off below 1 MHz (the mask rolls off at 2 MHz). Jitter transfer compliance is essential in order to prevent jitter accumulation in a network, especially if it includes the use of repeaters.

Conclusion

This note has reviewed using the OmniBER718/725 to make jitter measurements of OC-48 transceivers in conjunction with different reference designs from AMCC and Vitesse. Jitter was defined and potential jitter sources were discussed. It is important to remember that jitter always manifest itself as phase variations, and careful design can help to minimise its impact.

Jitter specifications for SONET/SDH were reviewed for jitter generation, tolerance and transfer. Test procedures were applied using the OmniBER718/725 communications and jitter analyser and reference design boards. The main objective being to show the suitability of the OmniBER 718/725 for a typical application using OC48 Tranceivers with commercially available ICs and also to compare jitter performance against the SONET/SDH specification that applies to whole systems. Finally, results were discussed in order to establish their role and importance at system level.

To conclude, it is important to remember that jitter specifications apply to Network Elements and compliance of individual components alone does not guarantee that the whole system will fulfill the SONET/SDH requirements for jitter. Careful consideration and attention towards interconnect impedance of high speed signals will help to minimise jitter and improve system transmission quality.

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